REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Office Action of March 27, 2003 has been received and contents carefully reviewed.

By this amendment, Applicants hereby amend claims 3, 5, 7, 8, 10, 12, 13, 15, 17, and 19 for the sole purpose of satisfying the requirements of 35 U.S.C. § 112, first and second paragraphs and respectfully submit no new matter has been entered. Moreover, Applicants respectfully submit the present amendment does not raise new issues that would require further consideration and/or search.

In the Office Action, the Examiner objected to claims 5 and 12 under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim; rejected claims 1, 2, 4, 6, 8, 9, 11, and 20 under 35 U.S.C. § 102(e) as being anticipated by Shin (U.S. Pat. No. 6,323,836); rejected claims 3, 5, 7, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Nakano et al. (U.S. Pat. No. 6,229,513); and rejected claims 13-19 under 35 U.S.C. § 103(a) as being unpatentable over Nakano et al. in view of the Related Art shown in Figure 3. The rejection of these claims is traversed and reconsideration of the claims is respectfully requested in view of the following amendment and remarks.

Preliminarily, it is noted that while the Office Action Summary of the Office Action mailed March 27, 2003 states claim 21 is pending and is rejected, Applicants respectfully submit a rejection of claim 21 has not been set forth by the Examiner. Applicants respectfully submit claim 21 is allowable over the cited references.

The Examiner objected to claims 5 and 12 under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicants respectfully submit the aforementioned objection to claims 5 and 12 is moot in view of the amendment to claim 12.

The rejection of claims 1, 2, 4, 6, 8, 9, 11, and 20 under 35 U.S.C. § 102(e) as being anticipated by Shin is traversed and reconsideration is respectfully requested.

Independent claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "a timing controller... for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of said line memory to the driving circuit every period of the data clock... ." None of the cited references including Shin, singly or in combination, teaches or suggest at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 1 and claims 2-7, which depend therefrom are allowable over the cited references.

Independent claim 8 is allowable over the cited art in that claim 8 recites a combination of elements including, for example, "a timing controller... for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock... and for outputting the data in each of the groups to the driving circuit during each period of the input data clock." None of the cited references including Shin, singly or in combination, teaches or suggest at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 8 and claims 9-12, which depend therefrom are allowable over the cited references.

Independent claim 20 is allowable over the cited art in that claim 20 recites a combination of elements including, for example, "a data clock generating step of frequency-

dividing an input first data clock at a frequency-division ratio...; a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock..." None of the cited references including Shin, singly or in combination, teaches or suggest at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 20 and claim 21, which depends therefrom are allowable over the cited references.

The Examiner cites Shin as teaching "...a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every period of the data clock... (see column 5, line 18-column 6, line 18)."

Applicants respectfully submit that Shin does not teach or suggest any data that is outputted to the driving circuit every period of a received data clock.

For example, Applicants respectfully submit at column 5, lines 28-32, Shin teaches (with reference to Figure 7) "...driving circuit... includes a clock generator 200 having an input terminal for receiving a first clock signal CK1 and an output terminal for outputting a second clock signal CK2; a data controller 210 having an input signal terminal for receiving a data signal D and output terminals for outputting an odd video signal D1, ... an even video signal D2...; a plurality of odd data driver ICs 240 each having a ...data input terminal A1 connected to the odd video signal terminal D1...; and a plurality of even data driver ICs each having a ...data input terminal A2 connected to the odd video signal terminal D2..."

Further, Shin teaches at column 5, line 56 to column 6, line 18 (with reference to Figure 8) "...a first clock signal is applied. Then, the clock generator 200 produces the

second clock signal CK2, the period of which is twice that of the first clock signal CK1: i.e., the clock speed of the second clock signal CK2 is half that of the first clock signal CK1. According to the first clock signal CK1, the first odd data (video signal)d1 is stored in the odd memory 230a and the first even data (video signal)d2 is stored in the even memory 230b. According to the second clock signal CK2, the first odd data d1 and the first even data d2 are sent to the first odd data driver IC 240 and the first even data driver IC 250, respectively. At that time, the second odd data d3 is stored to the odd memory 230a, and the second even data d4 is stored to the even memory 230b according to the first clock signal CK1. The output of the first pair of data (d1 and d2) and the input of the second pair of data (d3 and d4) are performed at the same time. ...After the line data on the one-page data are latched at all the data driver ICs, all the latched data are sent to the data lines at one time".

Accordingly, Applicants respectfully submit the teachings of Shin are silent to the aforementioned combination of elements in the presently pending claims.

In the "Response to Arguments" section of the present Office Action, the Examiner states "...Shin does teach that the timing controller receives a clock signal CK1 from the exterior thereof, and generates a second clock signal CK2, which is outputted from the timing controller" and "...[t]he second clock signal CK2 is generated from the received data clock CK1, and data is output from the plurality of groups of the line memory (230) to the driving circuit every period of the data clock signal CK2 (see figure 8)."

Applicants respectfully submit, however, that the signal CK2 of Shin is a generated clock signal, not an exterior signal received by the timing controller. Signal CK1 of Shin is an exterior data clock signal received by the timing controller. Further, referring to Figure 8 of Shin, Applicants respectfully submit that while the data may be outputted to the driving

circuit every period second clock signal CK2, the data is not outputted during every period of the received data clock signal CK1. Rather, the data is outputted every other period of the received clock signal CK1. To reiterate, claim 1 includes, among other elements "a timing controller... for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of said line memory to the driving circuit every period of the data clock...", claim 8 includes, among other elements "a timing controller... for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock... and for outputting the data in each of the groups to the driving circuit during each period of the input data clock", and claim 20 includes, among other elements "a data clock generating step of frequency-dividing an input first data clock at a frequency-division ratio...; a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock..."

Accordingly, Applicants respectfully submit the teachings of Shin are silent to the aforementioned elements of the presently pending claims.

The rejection of claims 3, 5, 7, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Nakano et al. is traversed and reconsideration is respectfully requested.

Applicants respectfully submit that claims 3, 5, 7, 10, and 12 are allowable at least because these claims depend from independent claims 1 and 8, which are believed to be allowable.

The rejection of claims 13-19 under 35 U.S.C. § 103(a) as being unpatentable over Nakano et al. in view of the Related Art shown in Figure 3 is traversed and reconsideration is respectfully requested.

Independent claim 13 is allowable over the cited references in that claim 13 recites a combination of elements including, for example, "a line memory for receiving two pixel data unit sequentially from the exterior thereof and dividing the data for at least one line into a plurality of groups to store the divided data therein and for outputting the two pixel data unit from each of the groups; ...a timing controller... connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to generate a first data clock and for outputting the two pixel data in each of the groups to the driving circuit during each period of the first data clock..." None of the cited references including Nakano et al. or the Related Art shown in Figure 3, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that independent claim 13 and claims 14-17, which depend therefrom are allowable over the cited references.

Independent claim 18 is allowable over the cited references in that claim 18 recites a combination of elements including, for example, "a latch circuit for latching and outputting two pixel unit inputted from the exterior thereof; a driving circuit... connected to the latch circuit...; and a timing controller... connected to the latch circuit and the driving circuit, for receiving a data clock inputted from the exterior thereof to output each one pixel data to the driving circuit at a desired time interval during one period of the data clock." None of the cited references including Nakano et al. or the Related Art shown in Figure 3, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 18 and claim 19, which depends from claim 18, are allowable over the cited references.

The Examiner cites Nakano et al. as failing to "specifically teach that the memory receives two-pixel unit..." and states Nakano et al. "does... teach that the first and second memories (112, 113) stores display data of an amount corresponding to a total number (2n) of the drain signal lines (D) connected to two drain drivers (130)" and "with reference to a second embodiment, a liquid crystal display of higher resolution has two bus lines (134a, b) as display data bus lines, and drain drivers (130') are connected thereto (see column 7, lines 43-50).

Applicants respectfully submit that Nakano et al. teaches that "the first and second memories (112, 113) stores display data of an amount corresponding to a total number (2n) of the drain signal lines (D) connected to two drain drivers (130)" at column 7, lines 3-8. The alleged "second embodiment" of Nakano et al. cited by the Examiner at column 7, lines 43-50 that "a liquid crystal display of higher resolution has two bus lines (134a, b) as display data bus lines, and drain drivers (130') are connected thereto" is actually admitted conventional art. Specifically, at column 3, lines 41-45 in the BRIEF DESCRIPTION OF THE DRAWINGS section, Nakano et al. states "FIG. 5A is a block diagram illustrating an exemplary approach, considered by the present inventors and others, for transmitting a display data from the display control unit to drain drivers..." At column 7, line 58 – column 8, line 2, Nakano et al. states "The approach illustrated in FIGS. 5A, 5B, however, requires a twice wider bus width for the display data bus line..., thereby causing an increase in the number of pins required for the display control unit 110, an increase in the number of layers and the area of the printed wiring board, on which the display control unit 110 is mounted. This further leads to an increase cost for the display control unit 110 and the associated printed wiring board, and a larger size of a connector attached to the printed wiring board..."

At column 8, lines 3-15 Nakano et al. states "According to this embodiment, however, since the frequency of the clock signal for latching display data can be lowered... only by adding a signal line for the clock signal D4 or ...D5 without the need for increasing the bus width of the display data bus line 134, it is possible to avoid an increase in the number of pins required for the display control unit 110..."

Accordingly, Applicants respectfully submit the "second embodiment" cited by the Examiner actually teaches away from the invention taught by Nakano et al. at column 4, line 32-column 7, line 42 and therefore cannot be combined with the invention taught by Nakano et al. at column 4, line 32-column 7, line 42 to arrive at the combination of elements in the present invention. Moreover, the Examiner has provided no motivation why one of ordinary skill in the art would be motivated to combine the teachings of the two embodiments and arrive at the claimed invention. Further, Applicants respectfully submit the Related art shown in Figure 3 does not cure the aforementioned deficiencies of Nakano et al.

Applicants believe the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

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